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# A FIVE ADDRESS, THREE OPERATION CARD PROGRAMMED CALCULATOR

by

Ralph Hafner and Robert L. LaFara

Copy Ma. B. L.

Presented by

K. L. Melsen

at the

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#### PORTHUMARY DATA

This is an informal report and is transmitted for information only. The data presented are tentalive and subject to later section.

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# U. S. NAVAL ORDNANCE PLANT Indianapolis 18, Indiana

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### A FIVE ADDRESS, THREE OPERATION CARD PROGRAMMED CALCULATOR

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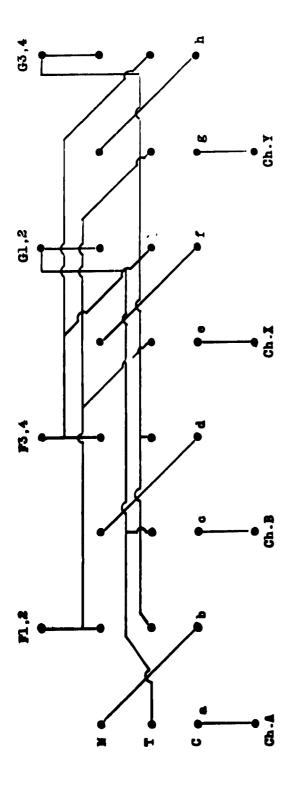
Ralph Hainer and Robert L. LaFara

This paper presents a complete description of the wiring and operation of five-address control panels for the Model II CPC.

#### A FIVE ADDRESS, THREE OPERATION CARD PROGRAMMED CALCULATOR

Addition, subtraction, multiplication and division of two eight-digit factors can be completed in much less than the normal calculate time allotted to the 605 calculator during a CPC card cycle. It would be desirable, therefore, to do more than one operation on more than two factors during a single card cycle. Since the CPC is basically a three address machine, this would seem impossible; however, five address control panels may be wired for the Model II CPC which will have the following features:

- 1. Eight 8-digit counters available on all four input channels. Eight digit factors from cards available on all four input channels.
- 2. Factors from 941 storage available on any two of the four input channels.
- 3. Three operations available in two different orders.
- 4. Table look-up with linear interpolation.
- 5. Special functions.
- 1. For convenience, let us call the two additional addresses channel I and channel Y. In order to have the first feature listed, the exits of the eight counter groupings are chain wired through selectors to the entries of channel A and with another chain to channel B; this wiring is done in the normal fashion. The counter exits are also wired into the field selector transfer hubs. The field selector is picked up by the channel I code to gate the proper counter or card columns to the calculator at read-in time. Another chain of selectors, which is controlled by the channel Y code is also used to gate a counter or card columns to the calculator. The field selector is used for channel I counter wiring in order to have co-selectors left 'or what is called channel interchange.
- 2. Normally, the channel A hubs are connected to factor storage 1 and 2, channel B hubs to factor storage 3 and 4, the commons of the field selector (which might be called the channel X hubs) to general storage 1 and 2, and the last commons of the channel Y chain to general storage 3 and 4. In order to read numbers from 941 storage to general storage in the calculator (feature 2 listed above) the channel A hubs are wired through selectors so that they may be read into any one of three places in the calculator; Fl,2; Gl,2; G3,4. If channel A is selected to read into Gl. 2 then the channel I data instead of reading into Gl. 2 is read into Fl.S; likewise, if data is read from channel A into G3.4, then the channel Y data is read into Fl.2. The channel B hubs are selected in a similar fashion. In programming, care must be taken that channel A and B data are not sent to the same place. Figure one shows the wiring of one position for channel interchange. The read-in impulses must also be selected through these selectors in case that it is desired to use a number already in the calculator when interchanging channels.



a and e are picked up by a code to interchange A and X b and g are picked up by a code to interchange A and Y c and f are picked up by a code to interchange B and X d and h are picked up by a code to interchange B and Y

FIGURE 1. Channel Interchange Wiring

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3. In the calculator, one program sweep is used for multiple operations. The programming for add, subtract, multiply and divide only takes sixteen program steps and hence may be wired three times on the 605 control panel. The following is the programming of the multiple operation sweep.

Operation	Step	R.O.	R.I.		Notes
All Add, Sub Mult Mult Mult Mult Mult Mult Div Div Div	1 2 3 4 5 6 7 8 9 10 11 12 13	F12RO F34RO ECRO ECRR F34RO F12RO ECRR F34RO F34RO F34RO F34RO MORO	ECRI+ See Note 2 F12RI MQRI Mult+ MQRI F12RI Mult+ Div F12RI ECRI+ F12RI	See Note 1 Ri 3rd Ro 6th Ro 6th	1. Ri 3rd on add & sub; Ri 5th on div; Ri 1st on mult.  2. ECRI+ on add; ECRI- on sub.  3. Ri 6th on div.  4. Normally F12RO; G12RO when order of operations is changed.  5. Normally G12RO; G3+RO when order of operations is changed.  6. Normally F12RI; G12RI when order
Div Div, Mult All All All Add, Sub Mult Mult Mult Mult Mult	14 15 16 17 18 19 20 21 22 24 25 26	F34RO MQRO F18RO 1/8 edj.  BGRR See Note 4 See Note 5 BGRO BGRR See Note 5 See Note 4 BGRR	Div  BCRI+  BCRI+  Fl&RI  BCRI+  See Note &  MQRI  MUlt+  MQRI  See Note 6	Reset  See Note 3 Ri 2nd  Ro 3rd See Note 1 Ri 3rd Rc 6th	of operations is changed.  7. Normally F12RI; G34RI when order of operations is changed.

Operation	Step	R.O.	R.I.		Notes
Div Div	28 29	See Note 5	Div See Note 6		1. Ri 3rd on add & sub; Ri 5th on div; Ri 1st on
Div Div	30 31	See Note 4	ECRI+ See Note 6	Ri 6th	mult.  2. ECRI+ on add;
Div	32	See Note 5	Div	Reset	ECRI- on sub.  3. Ri 6th on div.
Div Div,Mult	33 34	MQRO See Note 4	ECRI+	See Note 3	4. Normally F12RO; G12RO when order
All	35 36	1/2 adj.		Ri 2nd	of operations is changed.
A11	37 38	BCRR F12RO	See Note 7 BCRI+	Ro 3rd See Note 1	5. Normally G12RO; G34RO when order of operations
Add,Sub Mult	39 40	G34RO MCRO	See Note 2 Fl2RI	Ri 3rd Ro 6th	is changed.  6. Normally Fl2RI; Gl2RI when order
Mult Mult	41	BCRR G34RO	MQRI Mult+		of operations is changed. 7. Normally F12RI;
Mult	43	F12RO BORR	MQRI F18RI	Ro 6th	G34RI when order of operations is changed.
Mult Div Div	45 46 47	G34RO G34RO BORR	Mult+ Div Fl&RI		
Div Div	48	F12RO MQRO	BCRI+ F1SRI	Ri 6th	
Div	50	G34RO	Div	Reset	
Div Div, Mult	51 52	MQRO F18RO	BORI+	See Note 3	
All	53 54	1/2 adj.		Ri 2nd	
All All	55 56	EGRO F18RO	Flari Glari	Ro 3rd	
All	57 58	F18RO F18RO	P34RI G34RI		

To summarize the calculator wiring, steps 2 through 17 perform operation one on the factors in F1,2 and F3,4. Step 19 transfers the answer back to F1,2. Steps 20 through 35 perform operation two on the previous result and what is in G1,2. Step 37 transfers this answer back to F1,2. Steps 38 through 53 perform operation three on the previous result and what is in G3,4. Steps 55 through 58 transfer the final answer back to F1,2; F3,4; G1,2; G3,4. This wiring permits all operations of the form [(A D B) D X] D Y = C; where D means operation one and may be add, subtract, multiply, or divide, likewise with D, D. There are 64 such possible operations and they are listed below.

A+B+X+Y	A-B+X+Y	AB+X+Y	A+B+X+Y
A+B+X-Y	A-3+X-Y	<b>AB+X-Y</b>	A+ B+X-Y
(A+B+X )Y	(A-B+X)Y	(AB+X)Y	(A+B+I)Y
(A+B+X)+Y	(A-B+X)+Y	(AB+X)+Y	(A+B+I)+Y
A+B-X+Y	A-B-X+Y	AB-X+Y	A+B-X+Y
A+B-X-Y	A-B-X-Y	AB-X-Y	A+B-X-Y
(A+B-X)Y	(A-E-X)Y	(AB-I)Y	(A+B-X)Y
(A+B-X)+Y	(A-B-I)+Y	(AB-I)+Y	(A+B-X)+Y
Y+X( E+A)	(A-B)X+Y	ABX+Y	(A+B)X+Y
Y-X(E+A)	(A-B)X-Y	ABI-Y	(A+B)X-Y
Y[X(B+A)]	(A-B)XY	ABXY	(A+B)XY
Y+[Z(E+A)]	(A-B)X+Y	ABZ+Y	Y+I(G+A)
Y+I+(E+A)	(A-B)+X+Y	AB+X+Y	(A+B)+X+Y
Y-X+(E+A)	(A-B)+X-Y	AB+X-Y	(A+B)+X-Y
[ (A+B)+X]Y	[A-B)+X]Y	(AB+I)Y	[ (A+B)+I]Y
[ (A+B)+X]+Y	[(A-B)+X]+Y	(AB+I)+Y	[ (A+B)+X]+Y

It would be very desirable if the parentheses could be rearranged so that operations like AB+XY could be performed (feature 3). This may be done by picking up a calculate selector which changes the programming such that F18RO is replaced by G18RO on steps 80, 85, 30, and 34; G18RO is replaced by G34RO on steps 81, 84, 87, 88, and 38; F18RI is replaced by G18RI on steps 88, 86, 89, and 31; and F18RI is replaced by G34RI on steps 88, 86, 89, and 31; and F18RI is replaced by G34RI on step 37. This changes steps 80 through 35 so they perform operation two on the factors in G1,8 and G3,4. Step 37 transfers this answer into G3,4 so that steps 38 through 55 perform

operation 3 on the result of steps 2 through 17 and the result of steps 20 through 35. This permits all operations of the form (A(1)B)(3) (X(2)Y); there are 64 such operations but 32 of these are duplicates of the previously mentioned ones. Due to scaling difficulties, it may be desirable to use one order in preference to another. For example, A+B+X+Y is equivalent to (A+B)+(X+Y) but if A=4, B=3, X=6 and Y=-5 the wrong answer will result if the first method is used since one of the partial answers would exceed 10. The 32 operations which are not duplicates of the above are listed below.

(A+B)+XY	(A-B)+XY	AB+XY	(A+B)+XY
(A+B)+(X+Y)	(A-B)+(I+Y)	AB+(X+Y)	(A+B)+(X+Y)
(A+B)-XY	(A-B)-XY	AB-XY	(A+B)-XY
(A+B)-(X+Y)	(A-B)-(I+Y)	AB-(X+Y)	(A+B)-(X+Y)
(A+B)(X+Y)	(A-B)(X+Y)	AB(X+Y)	(A+B)(X+Y)
(A+B)(X-Y)	(A-B)(X-Y)	AB(X-Y)	(A+B)(X-Y)
(A+B)+(X+Y)	(A-B)+(X+Y)	AB+(X+Y)	(A+B)+(X+Y)
(A+B)+(X-Y)	(A-B)+(X-Y)	AB+(X-Y)	(A+B)+(X-Y)

4. The fourth feature of this board is table look-up with linear interpolation. If  $f(a_n)$  is the table function corresponding to the table argument  $a_n$ , then the formula for finding the function f(x) at the argument x, which is not necessarily a table entry, using linear interpolation is:

$$f(x) = f(a_n) + \left(\frac{x - a_n}{a_{n+1} - a_n}\right) [f(a_{n+1}) - f(a_n)].$$

When this formula is written in the form:

$$f(x) = (x - a_n) q_n + f(a_n)$$

where

$$Q_n = \frac{f(a_{n+1}) - f(a_n)}{a_{n+1} - a_n}$$

then it is easily seen that the operation is one of the form (A-B)X+Y=C.

This means that the entire operation may be performed on a single card cycle without taking any program cycles. The argument is read onto channel A and into counter 8 prior to running the table deck. The first table card has a special control punch which disconnects the negative balance test exit of counter 8 from its normal function and connects it to the pick-up of a selector by means of a latch selector which is not dropped out until the end of the table. The table must be arranged such that the arguments are always positive and in ascending order but they need not be spaced at equal intervals. The second table card reads the first table argument into counter 8 negatively and each card thereafter reads the difference between two successive arguments into counter 8 negatively. Counter 8 will go negative when the sum of the differences plus the first table argument exceeds the argument read in; then the negative test exit will give the impulse to pick up a selector, this selector emits the instructions for subtract, multiply, and add into the coding selectors for operation one, two, and three respectively. The cards are punched so that  $\mathbf{a}_n$  is in the card columns for entry onto channel B,  $Q_n$  is in the card columns for entry into channel X, and f(a,) is in the card columns for entry into channel Y; the difference  $\mathbf{e}_{n+3} = \mathbf{a}_{n+2}$  is entered in a special field from wh: h it is read into counter 8 negatively, it is displaced two cards as indicated by the subscripts in order that the timing comes out correctly. The argument x stays on channel A until the interpolation calculation is made. New information,  $a_n$ ,  $Q_n$ , and  $f(a_n)$  is read in on every card but is not used until the proper time. After the interpolation, the answer is read on to all channels but is erased from B, X, and Y when new data is read in. The last table card clears counter 8 and returns it to its normal function. At the end of the table, the answer is available on channel A.

5. Since the multiple operation wiring requires only one program sweep, there are two sweeps still available for other programming. One of these is used to compute special functions and is essentially the wiring described by Bill Heising in Technical Newsletter No. 5. The primary difference is that the number of terms necessary for  $\sin A$ ,  $\cos A$ ,  $\exp A$ ,  $\exp (-A)$ ,  $\sinh A$ , and  $\cosh A$  is predicted by the valculator instead of the programmer. This is done by evaluating the formula N=2|1.5|A|+11 where only the integral part of |1.5|A| is retained. In case N must be even, then N=2|1.5|A|+18. This is sufficient to assure that  $A^N/N! \leq 10^{-7}$ . The third program sweep has been kept free for temporary wiring of functions that are not needed frequently; as an example, this sweep has been used to compute the Bessel functions,  $J_n(A)$ , where n=0,1,2,3,4,5,6,7,8,9.

The channel C wiring is standard as well as most other wiring not specifically mentioned. Since this is a fixed decimal system, the high order positions of the electronic counter are wired into the compare unit to provide an overflow stop in case  $C \ge 10$ .

As an example of the savings afforded by the multiple operation system, consider the evaluation of the polynomial

$$y = ax^4 + bx^3 + ox^3 + dx + e$$
.

First re-write in the factored form:

$$y = \{ (ax + b) x + c | x + d \} x + e .$$

With a single operation, three address system, this would probably be performed in the following menner:

Card	No .	Operation			
1		<b>a</b> x		-	C,
2		<b>C</b> 1	+ b	-	C <sub>2</sub>
3		C,	x	-	C3
4		<b>C</b> 3	+ 0	-	04
5		C4	x	-	C
6		C <sub>B</sub>	+d	-	C <sub>e</sub>
7		C <sub>e</sub>	x	-	C,
8		q,	+ •	-	y

With the multiple operation system, provided numbers are allocated to storage properly, the computation would be done as follows:

The second second

Card No.

Operation

$$(\mathbf{ax} + \mathbf{b}) \mathbf{x} = \mathbf{C_1}$$

$$2 (C_1 + c)x + d = C_2$$

$$C_2 x + e = y$$

The above case is somewhat idealized since frequently intermediate answers must be stored. Furthermore, if all three operations are multiplications and/or divisions, the calculator may not have time to finish the calculation and will hold up the card feed resulting in a loss of time. On typical jobs, the multiple operation system increases the speed by a factor of one and one-half.

Actually, the number of selectors needed to wire the 418 control panel exceeds the number available. In wiring this board, some back circuits were included; however, the programmer could avoid these by remembering certain rules but this is clumsy. By adding ten selenium rectifiers to the machine, the back circuits were eliminated and some pilot selectors were freed for other purposes.

Prepared by

Ralph Horner

Mathematics Division

Approved by

L. Vielsen

Head, Mathematics Division

Robert L. LaFara Mathematics Division

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